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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,258	08/24/2001	James M. Derderian	4831US (01-0105)	2185

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/939,258	DERDERIAN, JAMES M.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-25,28-35,53 and 54* is/are pending in the application.

4a) Of the above claim(s) *9,24 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,10-23,25,28,30-35,53 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

In view of the appeal brief filed on 12-23-6 and newly discovered prior art, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 5-8, 10-17 and 53 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility.

In particular, the claim limitation, "resiliently compressible" is not supported by either a specific and substantial asserted utility or a well established utility.

Claims 1, 3, 5-8, 10-17 and 53 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention. Specifically, one skilled in the art clearly would not know how to use the resiliently compressible spacer.

Claim 25 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hikita (6724084) and Eldridge (6835898).

At column 11, lines 24-44; column 12, lines 28-33; column 12, line 53 to column 13, line 52; column 14, lines 3-18; column 14, line 60 to column 15, line 6; column 15, lines 27-39; column 18, line 34 to column 19, line 38; and column 20, lines 33-36, Hikita discloses the following:

A semiconductor device assembly, comprising: at least one semiconductor device 1; and at least one spacer BD protruding from a surface of the at least one semiconductor device, the at least one spacer inherently defining a distance the surface of the at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device; wherein the at least one spacer protrudes from an active surface of the at least one semiconductor device; comprising a plurality of spacers that are arranged to inherently stably support the another semiconductor device; the another semiconductor device positioned adjacent the at least one spacer, opposite from the at least one semiconductor device; adhesive

material 3 between the at least one semiconductor device and the another semiconductor device; wherein the adhesive material is located between adjacent spacers; wherein the at least one spacer comprises electrically conductive material; wherein the at least one spacer communicates with a "ground" plane of the at least one semiconductor device; a substrate 14 with which at least one semiconductor device is associated; wherein the substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads; wherein at least one bond pad 12 of the at least one semiconductor device is in communication with a corresponding contact area of the substrate; at least one discrete conductive element 13 extending from the at least one bond pad, over an active surface of the at least one semiconductor device, to the corresponding contact area; wherein the at least one spacer is secured to noncircuit bond pads 52 of the at least one semiconductor device; wherein the at least one spacer is secured to a contact pad 52 of the at least one semiconductor device.

A semiconductor device assembly, comprising: a substrate; a first semiconductor device associated with the substrate, bond pads of the first semiconductor device in communication with corresponding contact areas of the substrate; mutually laterally spaced discrete spacers positioned on and protruding from an active surface of the first semiconductor device, at least one spacer of the mutually laterally discrete spacers being in communication

with a "ground" or reference voltage plane of the first semiconductor device; and a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane; wherein the substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads; wherein the bond pads and the corresponding contact areas communicate by way of discrete conductive elements positioned therebetween; wherein the discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads; wherein the mutually laterally spaced discrete spacers are secured to noncircuit bond pads of the first semiconductor device; wherein the mutually laterally spaced discrete spacers comprise conductive material; wherein the mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of the first semiconductor device; wherein at least one of the mutually laterally spaced discrete spacers is inherently compressible; an adhesive layer between the first semiconductor device and the second semiconductor device; wherein at least some of the mutually laterally spaced discrete spacers extend through the adhesive layer; an encapsulant material 3 substantially covering the first semiconductor device, the second

semiconductor device, discrete conductive elements, and portions of the substrate located adjacent to the first semiconductor device; at least one external connective element 14 carried by the substrate and in electrical communication with at least one corresponding contact area of the substrate; wherein the at least one spacer is secured to a contact pad of at least one of the first semiconductor device and the second semiconductor device.

To further clarify the disclosure of the second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers, the at least one spacer establishing communication between the back side of the second semiconductor device and the ground or reference voltage plane, it is noted that the term "back" is a relative term, and the side of the second semiconductor device facing the active surface of the first semiconductor device is inherently at least the back (reverse) side relative to the side opposite the back side. To continue to afford applicant the benefit of compact prosecution, as evidenced by McFarland (20020074637), paragraph 18, the scope of the term "back side" is not limited to the non-active side of a semiconductor device.

However, Nikita does not appear to explicitly disclose resiliently compressible spacers.

Nonetheless, at column 58, lines 31-43; column 59, lines 24-28 and 38-51; column 59, line 62 to column 60, line 8; column 61, lines 23-34; column 62, lines 26-41; column 77, lines 8-45; column 97, line 66 to column 98, line 18; column 132, line 66 to column 133, line 12; and column 133, line 41 to column 134, line 176, Eldridge discloses resiliently compressible spacers "contact structures." It would have been obvious to combine this disclosure of Eldridge with the disclosure of Hikita by substituting or combining the spacers of Eldridge for or with the spacers of Hikita because, as disclosed by Eldridge as cited, because the spacers have high aspect (height:width) ratios, cleaning (e.g., of solder flux) and inspectability would be increased, as compared with traditional solder-bump type flip-chip surface mount processes, such as the spacers of Hikita; the same spacers can be used for demountable or permanent attachment of the electronic component; the spacers can be used as a standard means of interconnect between substrates and components which have matching patterns of terminals; the self-planarizing feature of the spacers (i.e., resilient spacers originating from different levels can all be made to terminate in a common plane) affords many opportunities not present with prior art interconnection techniques; the spacers can be bonded to a terminal that is skewed with respect to other terminals; the spacers have high electrical conductivity (low resistivity) in order that constriction resistance and bulk resistance are low;

the spacers have high thermal conductivity so that joule heat (I^2 R) is rapidly conducted away from the spacers interface; the spacers have softness, so that a-spots are large, thereby providing low constriction resistance; the spacers have high hardness for low mechanical wear; the spacers have high strength to provide the ability to serve as a spacer and cantilever beam to give low mechanical wear; the spacers have high noble metal content for extended shelf life, low electrical noise and excellent reliability; the spacers have the ability to form extremely thin lubricating films, but not an excess of frictional polymer; and the spacers have low cost.

Also, Hikita and Eldridge does not appear to explicitly disclose wherein heights of the at least one resiliently compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

Notwithstanding, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, **in view of the applied prior art**, the dimensions are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere

dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular **unobvious** purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 16, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita and Eldridge as applied to claims 15 and 18, and further in combination with Pu (6593662).

Hikita and Eldridge do not appear to explicitly disclose wherein heights of the at least one resiliently compressible spacer exceeds a maximum height the at least one discrete conductive element protrudes above the active surface.

Still, at column 1, lines 25-48; column 2, lines 17-20 and 30-42; and column 3, line 66 to column 5, line 32, Pu discloses wherein heights of at least one spacer 204b, 220, 204c exceeds a maximum height an at least one discrete conductive element 210a protrudes above a surface 201. It would have been obvious to combine this disclosure of Pu with the disclosure of Hikita and Eldridge because, as disclosed by Pu, it would facilitate provision of a stacked-die package structure capable of stacking dies having

substantially the same size and bonding pads around the peripheral sides of the dies.

Also, Hikita and Eldridge do not appear to explicitly disclose wherein bond pads of the second semiconductor device communicate with the corresponding contact areas of the substrate by way of discrete conductive elements positioned therebetween; at least one additional semiconductor device positioned over the second semiconductor device.

Regardless, as cited, Pu discloses wherein bond pads 222 of a second semiconductor device 208 communicate with corresponding contact areas of a substrate 202 by way of discrete conductive elements 210b positioned therebetween. 33. (Previously presented) The semiconductor device assembly of claim 18, further comprising: at least one additional semiconductor device "a number of dies" positioned over the second semiconductor device. It would have been obvious to combine this disclosure of Pu with the disclosure of Hikita and Eldridge because it would facilitate provision of a stacked-die package structure capable of stacking a number of dies having substantially the same size and bonding pads around the peripheral sides of the dies.

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
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14-Jan-07

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01/22/07